A Different Approach to Implement an Active Input Current Shaper

Introduction.

Several topologies have been recently proposed in order to search an ac/dc converters with high efficiency, small size and fast regulation of the output voltage complying with harmonic standard specifications. The purpose of just meet the standard specifications is due to the cost, the ac/dc conversion is made trying to obtain the lowest cost as it is possible. An option to obtain a good efficiency, a fast regulation as well as comply with standard specifications is to use the active input current shaping technique [1-7].

The active input current shaping technique consists of one converter with two outputs: the main output is used to feed the load, the auxiliary output is used to shape the input current (Fig 1). The auxiliary output is connected in series with the rectified ac mains, this topology has been studied extensively in the literature, and many variations have been proposed [4-7].

In this paper a new active input current shaper (AICS) is presented, the parallel scheme. The scheme consists of one converter with two outputs: the main output feeds to the load, and the auxiliary output shapes the input current. But the auxiliary output is connected in parallel with the rectified ac mains (Fig 2).

The proposed parallel scheme can be extrapolated to many variations as there are on the series scheme, and some extrapolations will be shown. The new scheme is operated in continuos conduction mode in order to have a low dc bus voltage and low semiconductor current stresses.

In the next section the proposed scheme is studied, and some variations of the proposed scheme will be presented; in section three the simulation results are presented; and finally the conclusions are presented.

Proposed Scheme.

In order to understand the proposed scheme, first a brief analysis of the series AICS will be discussed. A simple configuration of the series AICS is shown in Fig 3.a, this scheme is used as benchmark. The main output operates as a flyback converter and the auxiliary output operates as a forward converter. To understand the operation of the shaping technique, the auxiliary output is modeled as a pulsating voltage source (Fig 3.b). The series AICS operates as follows:

- If the rectified ac mains voltage is higher than the capacitor voltage minus the pulsating voltage source ($V_r > V_c-V_p$), then the inductor $L_1$ is charging.

- ...
If the rectified ac mains voltage is lower than the capacitor voltage minus the pulsating voltage source (\(V_r < V_c - V_p\)), then the inductor \(L_1\) is discharging or with zero current if even there is no stored energy.

With this technique the full bridge diode is obligated to conduct a little more of time that the traditional one plus a bulky capacitor. This permits that the harmonic content of the line current becomes lower, so the standard specifications like the IEC-61000-3-6 is fulfilled.

To understand the proposed parallel scheme in this paper, the auxiliary output is also modeled as a pulsating voltage source, but with a diode is connected in series with this voltage source (Fig 4.a). It is important to notice that even for modeling purposes a diode is added, the final circuit has fewer semiconductors than the series AICS.

The parallel AICS operates as follows:

- If the pulsating voltage source is higher than the capacitor voltage, then the inductor \(L_1\) is charging \((V_p > V_c)\).
- If the pulsating voltage source is lower than the rectified ac mains voltage, then the inductor \(L_1\) is discharging \((V_p < V_r)\).

With this operation form the diode full bridge is obligated to conduct a similar time. This permits that the standard specifications like the IEC-61000-3-6 can be easily fulfilled.

The proposed parallel AICS circuit is shown in Fig 4.b. A small inductor was added to the pulsating voltage source to permit that the diode full bridge and diode \(D_1\) start and finish to conduct at zero current. Then no fast recovery diodes are required.
**Regulating the output voltage**

To produce a regulated output voltage is used the main output. In fig 4.b is used a Flyback converter, as this converter is fed by the bulky capacitor voltage (Vc) that is almost a constant voltage, and the output voltage is constant then the duty cycle is practically constant.

A voltage loop is used to regulate the output voltage, and it is not necessary an extra loop to shape the input current since the converter naturally demands a current with low harmonic content.

\[ u = K_p \cdot e + K_i \cdot \int e \, dt \]  

(1)

where:

- \( K_p \) = The proportional constant.
- \( K_i \) = The integral constant.
- \( e \) = The error voltage.

**Power processing**

The series AICS handles more power than if it was working as a standard converter. This is because the auxiliary output recycle an amount of power; the power flow diagram of the series AICS is shown in fig. 5. The parallel scheme also recycles energy, and the same power flow representation can also be used, but the difference is the amount of power recycled.

According to Fig 5 the percentage of the power delivered by the rectified ac mains (Pr) to the bulky capacitor is determined by:

\[ \frac{P_r}{P_c} = \frac{P_r}{P_p + P_r} = \frac{1}{\frac{P_p}{P_r} + 1} \]  

(2)

where:

- \( P_r \) = Power delivered by Vr
- \( P_p \) = Power delivered by Vp

The ratio \( \frac{P_p}{P_r} \) determines the amount of power recycled, which is if the ratio becomes lower then the power recycled becomes lower. Then it is important to minimize that radio in order to process less the energy, and then obtain a better efficiency.

The power recycled for the series AICS depends on the auxiliary output, represented for Vp according to the simplified circuit (Fig 4.a). As the pulsating voltage source and the rectified ac mains are in series the power delivered to the bulky capacitor (Cb) is a contribution of both sources. The power delivered for each

![Fig 5. Power flow representation for AICS schemes.](image)

![Fig 6. The parallel AICS with two terminals or auto-transformer](image)
voltage source is: \[ P_r = V_r * i_{L1} \] (3)
\[ P_p = V_p * i_{L1} \] (4)

With (3) and (4) the ratio for the series AICS is: \[ \frac{V_p}{V_r} \] (5)

The power recycled for the parallel AICS also depends on the auxiliary output, represented by \( V_p \) according to the simplified circuit (Fig 3.b). The pulsating voltage source and the rectified ac mains are in parallel, and the power contribution to the bulky capacitor (\( C_b \)) depends on the duty cycle. Then power delivered for each voltage source is: \[ P_r = V_r * i_{L1} * (1 - d) \] (6)
\[ P_p = V_p * i_{L1} * d \] (7)

With (6) and (7) the ratio for the parallel AICS is: \[ \frac{V_p}{V_r} * \frac{d}{1 - d} \] (8)

As can be observed in (5) and (8), the difference between the ratio is the term \( \frac{d}{1 - d} \). So if the duty cycle is lower than 0.5 the parallel scheme process less energy than the series scheme, and this term can be chosen by design. It is also important to notice the power recycled can be also minimized with the pulsating voltage source (\( V_p \)).

**Variations of the proposed converter.**

Many variations of the series AICS have been reported in literature [4-7]. These variations can also be implemented in the parallel scheme. The parallel can be extrapolated to a cell of two terminals like in Fig. 6. It can be modified the main converter, can also be used a symmetrically driven transformer to increase the switching frequency and obtain a small converter like in [4], and so with all variations reported in literature.

**Simulations results**

The converter was designed with the following parameters: \( P_o = 50W \), \( V_{in}=120Vac \), \( V_o=50Vdc \), \( L=1.4\mu H \), \( C_b=47\mu F \). The converter was designed to fulfill the IEC 1000-3-2 class D, since this is more restrictive than class A. Some simulation results of the converter are shown in Figs 7 through 10, the ac mains voltage and current are shown in Fig 7, a small EMI filter is used. In Fig 8 the rectified ac mains, and
the bulky capacitor voltage are shown.

In fig 9 the harmonic content vs the standard specifications IEC 1000-3-2 is shown, as can be observed the specifications class D is fulfilled. In fig 10 the harmonic content of the series AICS with the parallel AICS is compared at the same conditions, as can be observed the harmonic content is lower with the proposed scheme.

**Conclusions**

In this paper a new active input current shaper (AICS) is presented, the parallel scheme. In difference with the traditional series AICS, the proposed scheme connects the auxiliary output of the main converter in parallel of the rectified ac mains. This permits to process the power less than the series scheme, expecting better efficiency and a lower dc bus voltage. The parallel scheme proposed demand a current with a low harmonic content that the standard specifications and also than the series AICS. The parallel scheme can be extrapolated to all variations reported in literature to the series scheme.

The analysis, operations and simulations of the proposed scheme are presented. Also a brief comparison between the series AICS and the parallel AICS is presented. In the final version the complete analysis and experimental results of the parallel converter will be presented and the comparison with the series scheme.

**References.**


