Analysis of the Effects of Single Event Transients on an SAR-ADC based on Charge Redistribution

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Abstract—This work presents a study on the effects of Single Event Transients on SAR A/D converters based on charge redistribution. The effects of SETs are analyzed considering the worst-case pulses for the 130nm CMOS process. In this work, the fault injection is concentrated on the switches of the capacitor array of the studied converter. Preliminary results show that the transient effects may change the state of one or more bits of conversion. This is due to the fact that the affected stage may propagate an incorrect value to the remainder of the conversion, leading to multiple bit errors on the converted data. Moreover, a SET occurring on the switch connected to the common node of the capacitors may lead to an incorrect behavior that cannot be attenuated with the increasing on the sizing of the transistors, which suggests that additional fault tolerance techniques may be needed.

Keywords—SAR; charge redistribution; SETs; transmission gate switches; Analog-to-Digital Converter.

I. INTRODUCTION

Successive Approximation Register (SAR) A/D (Analog to Digital) converters based on charge redistribution are frequently used when area and power consumption are the most important factors for the design of the converter on the integrated circuit [1]. SAR ADCs are sequential converters that take N clock cycles to convert an analog input into an N-bit digital representation. They are frequently chosen over flash ADCs for medium to high-resolution applications, since flash ADCs over 10 bits are not commercially viable [2]. Additionally, SAR ADCs usually present better speed of conversion than Sigma-Delta [3], though the latter reaches higher resolutions than the former.

The low power feature of this kind of converter may be a desired benefit to critical applications as satellite control, instrumentation systems, and wireless sensor networks, for example. These applications may be subjected to environmental interactions, such as radiation effects and electromagnetic interference, and, despite that, it is desirable that the embedded converters perform well in such conditions.

Another motivation to study this kind of converter is that it is commonly present in programmable commercially available mixed-signal platforms, such as PSoC5 [4], SmartFusion [5] and MSP430F6638 [6]. Such kind of programmable mixed-signal (MS) circuits offer characteristics like fast prototyping, design flexibility and the reduction of the analog expertise level required from mixed-signal designers. For all these reasons, programmable analog and MS circuits have become an important platform to electronic systems design, including those oriented to critical applications, such as avionics and space systems, as well as nuclear and particle accelerator facilities.

It’s well known that ionizing radiation may affect the state of electronic circuits. An important class of radiation effects on electronic circuits is known as Single Event Effects (SEE). They may cause transient or permanent errors. In particular, this work consists on the simulation and analysis of the effects caused by one particular case of SEE known as Single Event Transients (SET) on an SAR converter based on charge redistribution.

Transient effects may be caused by the collection of charges on reversed biased P-N junctions of the semiconductor after a heavy ion strike or indirect ionization. At electrical level, these effects generate current pulses that may affect the MOS transistors, which may change the expected behavior of the circuit.

The basic building block of this type of converter is the capacitor array controlled by a set of switches. The effects of transient faults on programmable capacitor arrays were first addressed in [7]. Experimental results on a commercial SoC containing an SAR ADC based on charge redistribution are addressed on [8], where the simulations to explain the behavior observed experimentally on this type of converter was firstly idealized.

In this work, we analyze the faults that may occur on the circuit due to the injection of an SET on the analog switches of the converter. This is due to the fact that once the switch changes its state, it may change the subsequent steps of conversion, causing the results to be incorrect.

Fault injection was performed by Spice simulations, modeling the SETs as current sources attached to the drain of the transistors, according to the model developed by Messenger [6]. The results of the conversion are analyzed considering the worst-case scenario for the width and height of the current pulse, considering a predictive technology model (PTM) of the 130nm node.

This paper is organized as follows: Section II describes the basic topology for the SAR converter based on charge
redistribution. Section III explains the fault injection methodology, while section IV shows the obtained results. Finally, conclusions are presented on Section V.

II. MODELING OF THE CHARGE REDISTRIBUTION SAR CONVERTER ADOPTED

The design addressed in this work consists of a conventional implementation of a single-ended input, 8-bit SAR based on charge redistribution. This topology comprises three main building blocks: the capacitor array (consisting of one capacitor per bit and one additional capacitor), the switches, and the comparator, as can be seen in Fig. 1.

Besides these blocks, the converter also comprises a digital control part, which is not shown, for the sake of clarity.

The capacitor array consists of binary-weighted values of capacitances, so that the circuit may function like a binary-search algorithm.

An adaptation of the classical algorithm presented in [9], which describes the converter working principle, is as follows:

1) Sample – This step consists on the sampling of the signal from the input. This happens when the switch SA is connected to $V_{IN}$, switch SB is open, and switches S7 through S0 are connected to ground. The equivalent capacitor array will then retain a charge proportional to the input.

2) Hold –When the signal is sampled, it needs to be retained. The switch SB is closed, and switches S7 through S0 are connected to ground. The bottom-plate Sample & Hold circuit contained in this circuit, as presented in [9] suggests that the voltage at the bottom plates of the capacitors (common node of all capacitors) are held at the negative input of the comparator, according to Eq. (1).

$$V_{comp} = -V_{in}$$

(1)

In particular, when MOS switches are used, a negative voltage between the node and ground might turn the transistor back on, so we keep the voltage always positive pre-charging the common node of the capacitors with $V_{DD}$. The voltage $V_{DD}$ is added at this stage (Hold), and isn’t subtracted afterwards, since the switch SB is closed and it doesn’t open on the subsequent steps. The voltage $V_{DD}$ is cancelled from this node only at the output of the comparator by comparing the held voltage to $V_{DD}$ instead of 0V (ground), since $V_{comp} = V_{DD}$. Therefore, the voltage of the negative input of the comparator for this work is expressed on Eq. (2).

$$V_{comp} = V_{DD} - V_{in}$$

(2)

3) Charge Redistribution – The conversion itself starts at this step. The switch S7 is connected to the bus and the switch SA is connected to the full-scale range of the converter, denoted by $V_{REF}$, which is usually equal to $V_{DD}$. A capacitance divider is formed between C7 and the equivalent capacitance of the remaining capacitors that are in parallel (C6 through C0). This causes a value of $V_{REF}/2$ to appear at the negative input of the comparator added to the previous value of $V_{DD} - V_{in}$. The comparator will output a “high” value if $V_{in} > V_{REF}/2$, that is, if the MSB is “1”. If the output is “low”, the switch S7 is connected to ground, otherwise it is kept connected to the bus. This procedure follows with a comparison of each bit from $S6$ through $S0$.

For the current setup, the circuit that is simulated in this work comprises a unit capacitance of 12fF (i.e. the smaller capacitor). The switches built with MOS transistors use dimensions of $(W/L)_n = 260nm/130nm$ (ratio of 2/1) and $(W/L)_p = 520nm/130nm$ (ratio of 4/1) as well for the inverters used to obtain the complementary signals for the transmission gates.

In this work, the model used was the Predictive Technology Model (PTM) from Arizona State University [10]. In particular, we used the 130nm BSIM3v3 model for Bulk CMOS.
III. FAULT INJECTION

SETs were modeled as current sources using the double-exponential model developed by Messenger [11]. This method is used to perform the simulation of the effect of a collision between an ionizing particle and the MOS transistor. This effect may be simulated with the attachment of a current source between the drain of a transistor and ground on a sensitive node of the circuit when the drain junction of the transistor is reversed biased. This condition presents two situations: a pulse causing a “0-1-0” transition and a pulse causing an “1-0-1” transition depending on the condition of the transmission gate (ON or OFF) and the voltage between its terminals.

Fig. 3 shows the topology of the circuit adapted with the current source on the node of the S7 switch. The terminals of the current source will determine the type of transition of the SET (0-1-0 or 1-0-1).

![Fig. 3. Representation of the SET current pulse on the circuit on the switch S7.](image)

The method developed by Messenger consists on an analytical representation of a current pulse generated by an ion strike on the silicon as follows:

\[ I(t) = I_0 (e^{-t/\tau_1} - e^{-t/\tau_2}) \]  

(3)

The transient pulse modeled by Eq. (3) is governed by two exponentials, where the first one is dependent on the value of \( \tau_1 \) (collection-time constant of the junction) and the second one is dependent of the value of \( \tau_2 \) (ion-track establishment time constant). The parameter \( I_0 \) controls the peak current that is reached due the collision. The double exponential model can be modeled either on voltage or on current on SPICE using the command EXP.

The worst-case parameters for the SET pulse for 130nm technologies were measured experimentally in [12, 13]. The considered peak value of the SET is 2mA, as measured in [12] and the current pulse has a worst-case width of 700ps, as measured in [13]. It is important to use these values, because they are measured experimentally, providing the designers a way to prepare circuits of this technology node for harsh environments. The measurements usually differ between different technologies. We use \( t_{rise} \) of 10ps and \( t_{fall} \) of 200ps, as suggested in [14]. For this experiment, only the worst-case pulse width is tested. That is because the objective of this work is to get a better understanding on how the circuit will behave on extreme situations. Future works may include the study of shorter pulse widths, and shorter peak values – since the pulse width and the transient current peak may vary – to analyze a more realistic day-to-day scenario for this type of converter.

The effect of the pulse width is dependent of two main factors: the state of the transistor at the time the strike takes place, as well as the transistor sizing [14]. Another aspect to observe is that a wider pulse is created when a collision with an NMOS transistor occurs, since the collection depth of NMOS is bigger than PMOS, and, since usually we have a bigger drain area on the PMOS transistors, the effect on NMOS may be more prominent [15].

Fig. 4 shows the schematic of the equivalent circuit of the circuit on a redistribution stage with the proper connections to the transmission gates.

The switches chosen to be tested on this experiment were SA and SB; two switches from the MSBs (S7 and S5) and two switches from the LSBs (S4 and S2). The control signals for the switches were individually monitored to check for the appropriate transition to be injected (0-1-0 or 1-0-1).

On the first experiment, tests were conducted considering small switches \((W/L)_{SA} = 260\text{nm}/130\text{nm} \) (ratio of 2/1) and \((W/L)_{SB} = 520\text{nm}/130\text{nm} \) (ratio of 4/1). Then, the gate length of the transistors was systematically increased, according to the corresponding effect observed on the negative input and the output of the comparator.

![Fig. 4. Schematic of the equivalent circuit of the capacitor divider for the experiment.](image)

IV. RESULTS

The first experiment was conducted with faults being injected on the switch attached to the bottom plates of the capacitors (SB). Fig. 5 shows the signal of the input of the comparator when the SET occurs on the switch SB. The leftmost part of the image shows the input of the comparator when both signals overlap. The rightmost part of the image shows the error due the SET. It is clear to see that when the SET occurs, the subsequent stages of conversion fail.
It is important to observe that the signal affected by an SET on a SPICE simulation may exceed $V_{DD}$, since there’s no way to relate the amplitude of the current modelled by Messenger’s method to the voltage of the node on SPICE.

It was possible to observe that when the current pulse occurs on the switch SB, increasing the size of the switch will not cause any improvements against the SET effect, that is, the effect persists throughout all stages, propagating a wrong result to all posterior steps of the affected stage. This occurs because the voltage held on the bottom plate of the capacitors is leaked to ground.

Another experiment was conducted considering the switch S7. Fig. 6 shows the signal of the input of the comparator for an SET on the switch S7. Fig. 7 shows a zoomed window of the SET perceived at the input of the comparator.

Contrary to the switch SB, the effect is attenuated when the width of the switch is increased. The effect of the SET persist to cause a change of value on the results when the transistor sizing is increased up to $(W/L)_n = 39\mu m/130nm$ (ratio of 300/1) and $(W/L)_p = 78\mu m/130nm$ (ratio of 600/1). It’s important to observe that the transistors of the switches of the LSBs cannot have such large widths, because it would insert intolerable parasitic capacitance to the array, leading to misbalance on the charge redistribution step, and consequently, wrong converted results at the output.

Two additional experiments were conducted: a current pulse was attached to an LSB switch (S4) at an earlier stage of conversion (i.e. when the conversion was being performed on the MSB bit). The transient observed on the bus did not cause
any change on the conversion. This is due the fact that an LSB add a small fraction of voltage compared with the bus voltage on an earlier stage of conversion.

The second experiment on the switch S4 consists of applying a current pulse on the stage of conversion of the same bit. The same effect in switch S7 was observed on the switch S4. The images for the simulations comprising similar results presented earlier are omitted for the sake of simplicity.

As stated earlier, increasing the size of a LSB switch will give wrong results at the output. Redundancy techniques may be used to address this issue.

Another important factor that was possible to observe is that, since the SAR is a sequential converter, the earlier the SET occurs on the conversion, the higher will be the probability of more bits of the result with an incorrect value. This is because more steps of conversion will be affected due to an incorrect value at the negative input of the comparator.

Future works will consider a random effect (i.e. a SET on a random node and random stage of conversion) of SETs on the circuit, as well as the use of redundancy to mitigate the failures on this type of converter.

![Fig. 7. A zoomed window of the SET due the change of state on switch S7.](image)

**V. CONCLUSION**

In this work, the effects of transient faults on SAR converters based on charge redistribution were analyzed. Four main conclusions were observed.

The switches attached to the top plates of the capacitors are affected mainly when the transistors are sized with a small width. Once the pulse occurs, all the subsequent steps of conversion fail to recover.

If a switch from the LSBs is switched to the bus due to a current pulse on an early stage of conversion (i.e. when the converter is performing a conversion on the MSBs), the effect will not cause the converter to give wrong results at the output.

An SET affecting the switch SB has high impact on the results of the converter, since increasing the width of the switch will not cause the mitigation of the problem. This problem may be mitigated using fault tolerance techniques, such as redundancy of the switches.

Multiple bit errors may occur on the digital output of the converter. This effect happens mainly when the SET affects an early stage of the conversion. Due to the sequential nature of operation of this type of converter, whenever a SET occurs on an early stage of conversion, there is a probability that more than one bit of the latter stages will be incorrect. This conclusion is coherent with the results measured experimentally on the literature.

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