ON RELIABILITY ENHANCEMENT
USING ADAPTIVE CORE VOLTAGE SCALING
AND VARIATIONS ON NANOSCALE FPGAS

Petr Pfeifer, Zdenek Pliva
FM ITE, Technical University of Liberec,
Studentska 2/1402, Liberec, Czech Republic
email: {petr.pfeifer, zdenek.pliva}@tul.cz

Pieter Weckx, Ben Kaczer
IMEC, DRE
Kapeldreef 75, B-3001 Leuven, Belgium
email: fweckx, kaczer@imec.be

Abstract - Rapidly growing portfolio of new technologies in design and manufacturing of advanced integrated circuits allow higher integration of complex structures in ultra-high nano-scale densities. However, the real new devices are sensitive subjects to unacceptable effects of changes of the internal nanostructures. Changes in parameters due to process variations or device aging along the working or its life-time can result in significant in large timing variations or critical BTI-induced delays and may affect the final design quality and dependability, may result in delay faults, up to the device or equipment malfunction or failure. Also power supply voltage or temperature variations do typically result in significant changes of timing parameters. The presented and tested circuit, method and approach allows extremely simple control of the core voltage during critical operations or during the device lifetime. This paper include also key results of measurement of selected low-power programmable device manufactured using 28 nm low-power TSMC process, a brief comparison to the previous 45 nm LP technology node, as well as a short prediction to the next 22 nm technology node. The presented approach, data and results can also be used in design of various dependable systems.

Keywords: nanoscale devices, FPGA, reliability, dependable systems, core voltage, delay fault, ageing, BTI

I. INTRODUCTION

The rapid scaling trend in the last two decades is amazing. There is a new technology node available every approximately 2 years, now in ultra-deep sub-micron technologies, very close to the expected physical limits in pure nanoscale space and without completely new kind of technologies. Together with memories and high-end processors, the FPGA (Field Programmable Gate Arrays) devices are one of the first members of the latest device portfolio of all technology leaders. Exactly these members are just within our scope, when we do study, measure or detect as many as possible types of changes in nanostructures, applied on various FPGA platforms. In one of our experiments, we are interested in the real effects of scaling of the programmable technologies and platforms to the overall system performance and possible impacts.

The rapidly shrinking electronic nanostructures and devices are subject to many changes, including the generally faced negative ones, caused by various physical and very complex mechanisms, like NBTI (Negative Bias Temperature Instability) or PBTI (Positive Bias Temperature Instability), TDDB (Time-Dependant Dielectric Breakdown) or HCI (Hot-Carrier Injection), etc. They affect the key parameters of CMOS structures, the most utilized technology for the last decades. These internal physical mechanisms typically result in negative changes in the gate threshold levels, while lowering the maximal drain current, cut-off frequency, and hence elongating the processing delays in the aging-affected circuits (compared to the original design). The quality of the gate oxides (or dielectric in general) and interconnects (electro-migration) can be affected as well. In case of dependable systems, the key parameter lies in the negative changes in delays of critical paths or noise. The system failures due to such negative effects must be avoided. Hence, all the critical changes have to be detected, in the ideal case the given or generally sufficient time before it might result in the system malfunction or failure.

In most of CMOS devices, the effect of increased power supply results in faster circuit and operations. This fact is widely used in modern devices, including mobile processor, etc. The principle of changing the core voltage is very simple and can be found in many sources since 1980’s. However the correct implementation in modern devices has to be tested properly. However doing our best, there is no any such solution and measurement results available from real tests performed on our 28 nm technologies, see [1], [2] and [3]. Some information can be found e.g. in [4],
interesting ideas and related results can be found e.g. in [7]. We have introduced the method used during the test e.g. in [5] and [6]. This paper presents a kind of overview of the first key results from application of very low-cost and extremely simple method. The methodology can be used in low-power as well as fast systems with CPU or FPGA devices, however it can also be used for easy and precise measurement and reliability assessment purposes, not only in the growing and very complex world of dependable systems.

II. THE EXPERIMENT - ADJUSTING THE CORE VOLTAGE

Today, there are two basic and generally used solutions allowing desired change in the (FPGA) core voltage. The first one is typically used in high-power high-end systems, like Virtex 7- based development boards. It is based on expensive fully programmable DC/DC power management systems and devices, like AVS systems from Texas Instruments in [8] or [9] for low-power systems, or many similar technologies, which are controlled by a dedicated bus or by a standard SMBus or similar I2C. The change of the FPGA core voltage can be done in very rich way, however it also typically requires special software or dedicated hardware IPs. The second approach is based on utilization of very simple DC/DC low-cost switches, while the desired change in power supply is achieved by a suitable simple resistor network or PWM (Pulse-Width Modulation) via selected single I/O pin. Naturally, the chosen or available I/O pin has to have selected proper constraints in the design system, and the involved I/O voltage rails at the utilized voltage domain or power bank must be set over the core voltage value. However, it is the very typical configuration, the I/O power voltage rails are typically set to 1.5V (DDR memories and systems), 1.8V (selected dedicated ports, PLLs, XDAC units, etc.), 2.5V (memories) or 3.3V (general I/Os and ports) respectively. The actual core voltage as well as core temperature or many other voltages can be measured by the internal dedicated units, like XADC unit in the modern 28 nm FPGAs (see e.g. [10] for more details). No any other devices are required at all.

Fig. 1 shows the tested DC/DC solution using Zedboard, generally available low-cost development platform with LP 28nm FPGA device. As tested on the Zedboard, the PWM frequency has to be far over 1 MHz. With 100 or 200 MHz base frequency and PWM generation using probabilistic approach, the resolution can be set easily below 5mV step with very low noise figures. The selected I/O pin (our case) or any dedicated PWM output has to be configured in OC/OD mode with just none or single series resistor. In case of push-pull output, the Xc point has to be connected to the selected I/O pin via at least 2 resistors, creating the desired conditions. The last tested solution was created using a series capacitor to the Xc point (the original series resistor remains). This latter solution isolates possible static levels at the I/O pin and is suitable for really critical systems where clock stop can cause problems. However, we have not met any problems during our tests using the simplest presented solution only.

It has to be also clearly mentioned here, that the used modern DC/DC converters do already incorporate many protection, self-checking and fault-detection mechanisms. E.g. in case of the presented device, the used MAXIM DC/DC converter was widely tested under various conditions and the output was automatically held at the given limits. Same behaviour was experienced in case of also widely used Texas Instruments’ similar solutions. It is not possible to damage the FPGA device by disconnecting or a short-circuit occurring at one of the referencing resistors. The connection of such advanced DC/DC power supply solutions and the presented method and approach creates really very robust product while keeping the costs very low.

III. MEASUREMENTS AND RESULTS

In our previous papers [5] and [6], we have introduced the new method and e.g. in [11] also results regarding ageing effects in FPGAs. Our method actively utilizes undersampling and BRAMs (block RAM units) in modern FPGAs. The data streams are processed by simple and fast algorithm and signal duty cycle or frequency within given Nyquist zone can be calculated very easily and precisely.

The following figure 2 shows the key results of our measurements of the timing parameters of the FPGA internal structures under relatively wide voltage variations. All the measurements utilized our new method for precise measurement of frequencies of the active ring oscillators having the structure presented in [5]. The core voltage was changed by a multi-turn micropotentiometer, connected to the on-board DC/DC supply. The core voltage was measured internally by the internal units, as well as checked externally by a standard multimeter unit. The performed results show, that 28 nm technology has introduced more than 20% process variation effects (s.c.time-zero variations)
in the device timing parameters, and also similar range of ageing-inducted delays, typically referenced at 85°C and 10 year timeframe in today’s manufacturer’s documents and also in FPGA development systems.

Figure 2. Measurement results and the critical uncovered space available for delay faults or mitigation of most of aging effects.

IV. DISCUSSION

The previous figure has shown an interesting overview of the measurements performed on 28 nm low-power devices, with respect to all the key recommended or absolute values, mentioned in Xilinx datasheets, line [3]. The surprising results showing that the discovered space available for advanced core voltage scaling or core voltage variation is over 20%, when still present within the permitted core voltage range. In addition, when the system allows its full operation just from 0.95V, one can gain additional 10% space. It is fully sufficient for most of the designs and systems. The voltage can be continuously increased all along the device lifetime, or just only during execution of critical operations.

The figure 3 shows that it makes really sense to utilize voltage scaling in the latest 28nm LP FPGA systems, because those are evidently much more sensitive to this factor that the previous corresponding technology node using 45nm LP technology. It is obvious, that the dependence of frequency to core voltage can be sufficiently precisely modelled using quadratic models, like the ones mentioned in the chart. However, the detail in the figure shows that for the core voltage value and the maximal frequency of the internal circuits can be used only very simple linear model. This fact can be very useful and successfully utilized in many systems.

Only 28 nm FPGA devices were available during our experiments, any new FPGA devices and development kits with smaller feature size will be available in late 2014 year. However thanks to our partners in IMEC, a first projection of the presented method and discovered FPGA behavior can be performed at least to the very next technology node. Figure 4 shows results measurements on just the very next generation 20 nm high-k/metal-gate and SiON planar transistor structures. It shows important technology comparison and it is obvious, that one can expect again increased sensitivity to voltage levels. The IMEC results also fully correspond to our measurements in term of the discussed quadratic dependence and models.

Figure 5 shows, that there is naturally introduced some increase in the total power dissipation by the core voltage upscale, however due to already high static power consumption caused by higher leakage currents in modern
nanostructures, the measured total power dissipation of all the systems was higher of 15 % only within the proposed core voltage band. This value and current overhead can be fully neglected, because the DC/DC power levels and rails must be designed to generate much higher current levels and suppress much higher current or load changes. In addition, the measured current overhead can be even same or lower, that the naturally created power consumption inducted just by the manufacturing processes and the process variations.

The performed tests clearly show, that the voltage variation up to 1,2V are fully recoverable in the structures and do not cause any measurable negative changes or degradation in the tested FPGAs. The tests performed on similar structures and technology in IMEC (Leuven, Belgium) showed serious troubles starting at 1,5V, fully in line with our prediction, based on quadratic extrapolation only! Voltages up to 1,3V obviously do create fully recovery-able stress effects, the proposed limit set to 1,1V creates sufficient space for the device speed increase while keeping the device in good condition and also fulfilling the absolute maximum ratings given by the device manufacturer (Xilinx, e.g. [3]).

V. CONCLUSION

We have presented extremely simple method and complex measurement results performed on real 28nm LP Zynq XC7Z020 device, allowing mitigation of process variations and aging effects in dependable systems. In addition, also a brief comparison to the previous low-power 45 nm technology node and results preformed on the new 20 nm technology node were presented as well. The results clearly show increased sensitivity of the technologies to the power voltage variations, creating strategic rooms for mitigation of increasing negative ageing effects.

The future is intended for detailed study of the already implemented as well as available new solutions and mechanism, their analyses, description, modelling, and better understanding. Our growing data bank is an important part of the final methodology and toolbox, allowing complete measurement of most of the today’s internal structures, their usage for special parameter-aware placement and routing of critical design parts, evaluation or estimation of the key reliability parameters with respect to the initial values or points, up to the key simple or complex continuous or on-demand reliability assessments tasks. The presented solution enables additional reliability enhancements with extremely low added costs. The proposed low number of additional devices positively affects the design’s final MTBF (Mean Time Between Failures) or MTTF (Mean Time To Failure) parameters, as the key reliability assessment outputs.

It is obvious, that the presented solution is very simple and contains very low number in added components, hence the overall equipment reliability, namely lambda parameter, cannot be negatively influenced, especially when using standard reliability assessment methodologies.

ACKNOWLEDGEMENT

The research is supported by the Student Grant Scheme (SGS) at the Technical University of Liberec, and co-financed by the Czech Ministry of Education, Youth and Sport. The work is also supported by the COST LD-13019 and the COST Action IC1103-Median programmes.

REFERENCES