INTEGRATED CIRCUITS - MEASUREMENT OF ELECTROMAGNETIC IMMUNITY

Ing. Edmundo Gatti
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<th>Publishing date</th>
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• IEC 62132-2

• Part 2: Measurement of radiated immunity –

• TEM-Cell and wideband TEM-Cell method

• IEC 62132-1

• Part 1: General conditions and definitions
The document describes general conditions required to obtain a quantitative measure of immunity of ICs in a uniform testing environment. The measurement results can be used for comparison or other purposes.

Measurement of the injected voltages and currents, together with the responses of the ICs tested at controlled conditions, yields information about the potential immunity of the IC to conducted and radiated RF disturbances in given application.
• ELECTROMAGNETIC COMPATIBILITY

• *Ability of a system or device to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment.*

• ELECTROMAGNETIC IMMUNITY

• *The ability of a system or device to perform without degradation in the presence of an electromagnetic disturbance.*
• A method for measuring the immunity to radiated electromagnetic disturbances to an Integrated Circuit (IC).

• IC is mounted on an IC Test Printed Circuit Board (PCB) clamped to a mating port cut in the top or bottom of a TEM cell or GTEM cell.
• Significant IC Changes

• All changes that may influence the electromagnetic immunity of an IC.

• Examples: Design changes, new manufacturer or process line, die-shrink, new package type, significant process change or any other change to the die to improve or fix the die performance.
• Ambient Conditions:

• *Ambient Temperature: 23 +/- 5 degrees C for repeatability because the RF-Immunity may vary with temperature.*

• *RF ambient: The level shall be at least 6 dB below the lowest immunity level to be tested against.*

• *RF-Immunity of the test set-up: all equipment used excluding the DUT has to be sufficiently immune such that will not influence test results.*
• IC specific considerations:

• *IC supply voltage*: as specified by the IC manufacturer with a tolerance of $\pm 5\%$.

• *Activity of IC*: attempts should be made to fully exercise all available functions that significantly contribute to reveal the immunity of the IC.
• Activity of IC:

• To improve the test speed, the IC may be put into a fixed mode of operation to allow the disturbance signal to be swept through the frequency band: 150 kHz – 1 GHz.

• Asynchronous modes of operation between the DUT and the RF disturbance may be more appropriate to represent real operating conditions.
• IC stimulation:

• Describe the parameters to be controlled in order to assure test repeatability for the particular IC function.

• If a programmable IC is to be tested, software that flows in a continuous loop shall be written to assure that measurements are repeatable and shall be documented in the test report.
• IC monitoring:

• *All relevant activity states without unintended feedback to the immunity performance.*

• IC stability:

• *IC shall be stable over time such that two measurements shall yield the same results within the expected variation of the measurement technique.*
• Verification:

• **DC output voltage:** voltage regulator.

• **Supply current:** cross current may increase due to change of threshold voltages.

• **Demodulated audio frequency signal**

• **Jitter:** time base, logic gate, AD/DA converters.
• Verification:

• *Spikes and glitches.*

• *System reset.*

• *System hang-up.*

• *Latch-up.*
• Verification:

• *As the response of the IC subjected to the RF immunity test is determined by its functions, the mode of operations and the criteria which to be met, no dedicated guidance can be given on the BEST response parameter to be observed.*
### Table 2 Frequency step size versus frequency range

<table>
<thead>
<tr>
<th>Frequency range [MHz]</th>
<th>0.15 - 1</th>
<th>1 - 100</th>
<th>100 - 1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear steps [MHz]</td>
<td>\leq 0.1</td>
<td>\leq 1</td>
<td>\leq 10</td>
</tr>
<tr>
<td>Logarithmic steps</td>
<td>\leq 5% increment</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Critical frequencies such as clock frequencies, system frequencies of RF devices etc. shall be tested using finer frequency steps agreed by the users of this procedure.
\[ P_{AM\text{-Peak}} = P_{CW\text{-Peak}} \]

and

\[ P_{AM} = P_{CW} \cdot \frac{2 + m^2}{2(1 + m)^2} \]

NOTE: For example: 80% AM modulation (m = 0.8) results in:
\[ P_{AM} = 0.407 \cdot P_{CW}, \quad m = \frac{(Max - Min)}{(Max + Min)} \]
• Dwell time: *The dwell time for each frequency step and modulation shall be typically 1 s or at least the time necessary for the DUT to respond, the measurement system to record.*

• Monitoring of the IC: *The specific test shall be performed considering all operational functions. The leveling of the test signal shall be controlled in a way that all critical reactions of the DUT will be sensed: hysteresis effects, reactions on level variations.*
• Immunity limits or levels:

• *As this standard describes measurement methods, no immunity test levels, criteria or limits are given.*

• *Limits in general depend upon the application and functional requirements.*
• Performance classes:

• **Class A:** all functions of the IC perform as designed during and after exposure to a disturbance.

• **Class B:** all functions of the IC perform as designed during exposure, however, one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain in Class A.
Performance classes:

- **Class C**: a function of the IC doesn’t perform as designed during exposure but returns automatically to normal operation after exposure is removed.

- **Class D**: a function of the IC doesn’t perform as designed during exposure and doesn’t return to normal operation until exposure is removed and the IC is reset by simple operation action (e.g.: put off supply...).
• Performance classes:

• **Class E**: one or more functions of an integrated circuit do not perform as designed during and after exposure and cannot be returned to proper operation.
• Interpretation of results:

• Comparison between ICs using the same test method.

• Comparison between different test methods.

• Correlation to module test methods.
<table>
<thead>
<tr>
<th>ITEM</th>
<th>IEC62132-2 (G-)TEM</th>
<th>IEC62132-3 BCI</th>
<th>IEC62132-4 DPI</th>
<th>IEC62132-5 Workbench</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of disturbances</td>
<td>Radiated</td>
<td>Conducted</td>
<td>Conducted</td>
<td>Conducted</td>
</tr>
<tr>
<td>Proposed frequency range</td>
<td>150 kHz to 1000 MHz</td>
<td>150 kHz to 1000 MHz</td>
<td>150 kHz to 1000 MHz</td>
<td>150 kHz to 1000 MHz</td>
</tr>
<tr>
<td>Frequency range extendable</td>
<td>Upwards, cell dependent</td>
<td>Downwards, current injection probe dependent</td>
<td>Upwards, injection network dependent</td>
<td>Not recommended</td>
</tr>
<tr>
<td>Measurement of disturbances</td>
<td>RF current</td>
<td>RF Forward Power</td>
<td>RF voltage</td>
<td></td>
</tr>
<tr>
<td>Dynamic</td>
<td></td>
<td>depends on RF-Power meter (min. 40 dB)</td>
<td>depends on test generator</td>
<td></td>
</tr>
<tr>
<td>Common-mode disturbances</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Differential disturbances</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>Single pin influencing</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td></td>
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<td>Multiple pin influencing</td>
<td>Yes</td>
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<td>No</td>
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<tr>
<td>- Comparison of IC's</td>
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<td></td>
</tr>
<tr>
<td>- Evaluation in application</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Verification of coupling</td>
<td>yes, via</td>
<td>yes, via</td>
<td>No</td>
<td></td>
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<tr>
<td>Application</td>
<td>yes, via measurement</td>
<td>yes, via measurement</td>
<td>No</td>
<td></td>
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<tr>
<td>-------------------------------------------------</td>
<td>-----------------------</td>
<td>-----------------------</td>
<td>----</td>
<td></td>
</tr>
<tr>
<td>Verification of coupling path</td>
<td>High</td>
<td>High</td>
<td></td>
<td></td>
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<tr>
<td>Reproducing of measurement; operator dependent</td>
<td>No</td>
<td>No</td>
<td></td>
<td></td>
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<tr>
<td>IC qualification</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Working in a shielded room or box</td>
<td>Yes</td>
<td>recommended, depends on power level (see national and international safety standards)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>IC immunity</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>- Drain/path analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- On-chip coupling (cross-talk)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
- IEC 62132-2
- Part 2: Measurement of Radiated Immunity
- TEM – Cell and wideband TEM – Cell method
• This procedure was developed using a 1 GHz TEM cell with a septum to floor spacing of 45 mm and a GTEM cell with average septum to floor spacing of 45 mm over the port area.

• Other cells may not produce identical responses but may be used for comparative measurements.

• The IC test board controls the geometry and orientation of the operating IC relative to the cell and eliminates any connecting leads within the cell.
E and H into the TEM CELL
The RF disturbance applied at the input to the TEM cell is related to the electromagnetic field by the distance between the septum and the IC as mounted on the IC test board:

\[ E = \frac{V}{h} \]

- \( E \) = field strength in [V/m] or [dBV/m]
- \( V \) = applied voltage [V] across the 50 Ω load
- \( h \) = height [m] between septum and the IC
• Rotating the IC test board in the four available orientations in the TEM cell will affect the sensitivity of the IC.

• Dependent upon the IC, the response parameters of the IC may be different; e.g. a change of current consumption, deterioration in the A/D, D/A performance, jitter, etc.

• The intent of this test method is to provide a quantitative measure of the RF immunity from ICs for comparison or other purposes.
• **It shall be fitted with a wall port sized to mate with the IC test board.**

• **It shall not exhibit higher order modes over the frequency range being measured.**

• **The frequency range is 150 kHz to the frequency of the first resonance of the lowest higher order mode ( < 2 GHz ) using a single a single cell.**

• **The VSWR shall be less than 1,5.**
TEM CELL

side view

measurement plane

b

3b/4

b/2

b/4

a/3

a

cross section

septum

Field points in the TEM Cell
TEM CELL

Diagram showing the components of a TEM cell:
- Personal computer & data acquisition
- Power supply
- RF signal generator
- Power meters
- Power amplifier
- Directional coupler
- 50-Ω load
- PCB
- DUT
- TEM cell
• The wideband TEM (GTEM) cell shall be fitted with a wall port sized to mate with the IC test board.

• The frequency range is from 150 kHz to the frequency of the first resonance of the lowest higher order mode, typically > 2 GHz.

• The VSWR shall be less than 1.5.

• It enables the proper evaluation of ICs that utilize clock frequencies above 1 GHz.
Field points in the GTEM 500
• A 50 Ω termination with a VSWR less than 1,1 and sufficient power handling capabilities is required for the TEM cell 50 Ω port not connected to the RF disturbance generator.

• The gain (or attenuation) of the RF disturbance generating equipment, without the TEM or GTEM cell, shall be known with a accuracy +/- 0,5 dB.

• The flatness shall remain within a 6 dB envelope.
• Test configuration:

• The test set-up shall met the requirements as described in IEC 62132-1.

• One of the TEM cell 50 Ω ports is terminated with a 50 Ω load.

• The remaining TEM cell or GTEM 50 Ω port is connected to the output port of the RF disturbance generator.
• **The IEC 62132 describes a 100 mm square PCB consisting of four metal layers.**

• **It will mate with the wall port on the test cell used.**

• **The PCB may also contain additional inner layers as required to accommodate signal and power routing.**
Strip of vias connecting layer 1 to layer 4 around the periphery of the board - min. spacing 2,5, recessed min. 5 mm from edge.

Tinned area of layer 1 - min. width 5,0 around the board periphery.

Holes at the corners are optional (3,2 dia. and 5,1 from board edge).
• **The DUT side that faces into the test cell, is dedicated to a ground plane layer that completes the TEM or GTEM cell wall over the port opening.**

• **No other conductors are allowed on this surface because they may act as additional radiators.**

• **The ground plane should extend under the DUT, where practical for the IC package type.**
0.2 vias connect DUT pin traces.

Ground plane extended below DUT. Note via connections to ground.

0.8 vias connect layer 1 with layer 4

0.8 vias connect layer 1 with layer 4

Additional signal layers may be added as necessary.

All additional components shall be on the side of the PCB opposite the DUT (layer 4) and inside the via perimeter.

Supply decoupling shall be referred to this part of the ground plane.
• The periphery of this ground plane layer shall be plated (tin, solder, gold) to facilitate contact to the edge of the wall port cut in the top or bottom of the test cell.

• The access wiring and other required components, such as crystals, shall be on or connected to the support side of this circuit board, the side that faces out from the test cell.

• Measurement ports shall be made available on this side, to measure certain parameter of IC.
Tinned edge

Layer 1 - ground
Layer 2 - power
Layer 3 - signal
Layer 4 - ground and / or signal

5 min
1.6 nominal
0.75 max

All non-ground layers shall be recessed min. 1.6 away from board edges.

(All dimensions are in mm)
# Table 1: Pin loading recommendations

<table>
<thead>
<tr>
<th>IC PIN TYPE</th>
<th>PIN LOADING</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog</strong></td>
<td></td>
</tr>
<tr>
<td>- Supply</td>
<td>As stated by the manufacturer (or as required)*</td>
</tr>
<tr>
<td>- Input</td>
<td>10 kΩ to ground (Vss) unless the IC is internally terminated</td>
</tr>
<tr>
<td>- Output Signal</td>
<td>10 kΩ to ground (Vss) unless the IC is internally terminated</td>
</tr>
<tr>
<td>- Output Power</td>
<td>Nominal loading as stated by the manufacturer</td>
</tr>
<tr>
<td><strong>Digital</strong></td>
<td></td>
</tr>
<tr>
<td>- Supply</td>
<td>As stated by the manufacturer (or as required)*</td>
</tr>
<tr>
<td>- Input</td>
<td>Ground (Vss) or 10 kΩ to supply (Vdd) if cannot ground, unless the IC is internally terminated</td>
</tr>
<tr>
<td>- Output</td>
<td>47 pF to ground (Vss)</td>
</tr>
<tr>
<td><strong>Control</strong></td>
<td></td>
</tr>
<tr>
<td>- Input</td>
<td>Ground (Vss) or 10 kΩ to supply (Vdd) if cannot ground, unless the IC is internally terminated</td>
</tr>
<tr>
<td>- Output</td>
<td>As stated by the manufacturer</td>
</tr>
<tr>
<td>- Bi-directional</td>
<td>47 pF to ground (Vss)</td>
</tr>
<tr>
<td>- Analogue</td>
<td>As stated by the manufacturer (or as required)*</td>
</tr>
</tbody>
</table>
• **Pins that do not fall into any of listed categories shall be loaded as functionally required and stated in the test report.**

• **If other values are more appropriate for a particular IC, they may be substituted and shall be stated in the test report.**

• **The loading by the IC response analysis equipment shall not affect the intended load characteristics.**
• Ambient Conditions: *The ambient RF noise level shall be verified to be at least 6 dB below the lowest immunity level to be applied. The DUT shall be installed in the test set-up, as used for testing but shall not be activated. A small dipole or optical field sensor can be used for field monitoring.*

• *If the ambient noise is excessive we must to use a shielded enclosure, and place the RF generator as close as possible to the TEM cell.*
TEM Cell Immunity Test Set-up

Fig. 1. TEM cell susceptibility measurement setup. The load at port B is $Z_L = 50 \, \Omega$. 

INTI
• **Operational check:** Energize the DUT and check to assure proper function of the device.

• **With the IC test board energized and the DUT being operated in the intended test mode, measure the immunity to RF over the desired frequency band by using the measurement equipment necessary to evaluate the IC response parameter considered.**

• **The sweep time should be much greater than the IC code loop execution time.**
TEM and GTEM Immunity Test Technique

• Four separate immunity measurements are performed resulting in two sets of data.

• The first measurement is made with the IC test board mounted in an arbitrary orientation in the cell wall.

• The second measurement is made with the IC test board rotated 90 degrees from the orientation in the first measurement.
• For each of the third and fourth measurements, the test board is rotated again to ensure immunity are measured from all four possible orientations.

• The four sets of data shall be documented in the test report.

• An IC test plan should be defined to precise specific IC test parameters and the responses considered. It should include which IC pins are to be tested and immunity acceptance criteria.
• **IC immunity acceptance levels are to be agreed upon between the manufacturers and the users of ICs.**

• **The IC immunity acceptance levels apply to measurements over the frequency range of 150 kHz to 1 GHz in units of dBV/m.**

• **As an alternative, the IC response parameter is allowed to vary between certain levels of acceptance.**
Fig. 2. Current filament with arbitrary shape inside the TEM cell.
RF Voltage induced on segment “m”

Fig. 3. Magnitude of the RF voltage induced on segment \( m \) with respect to the whole voltage \( V_{\text{ind}} \) induced on a package lead as a function of the length \( m \) and the height \( h \).
Effect of EMF phase rotation on RF Voltage induced in different pins

Fig. 4. Top view of a TEM cell with an arbitrary DUT on the inside.
Fig. 5. Connection of the opamp pads to the package leads. The unused terminals of the dual-in-line package are left unconnected.
Fig. 6. Schematic description of the direct injection of an RFI voltage $V_{RF}$ into the input terminal of a voltage follower opamp. The numbers that are placed close to the opamp terminals refer to the leads of the package inside which this opamp is housed as shown in Fig. 5.
Fig. 7. TEM cell top view with the opamp placed in two different orientations. (a) Transverse orientation. (b) Longitudinal orientation. $\varepsilon = 2.54$ mm, $w = 7.4$ mm.
Fig. 8. Voltage follower dc output offset voltage shift induced by EMI in the TEM cell IC susceptibility test (circles) and in the direct injection susceptibility tests (rectangles). In both cases, the RF source has a frequency of $f = 100\ \text{MHz}$.
Fig. 9. Voltage follower dc output offset voltage shift induced by EMI in the TEM cell IC susceptibility test (circles) and in the direct injection susceptibility tests (rectangles). In both cases, the RF source has a frequency of $f = 300$ MHz.
Fig. 10. Voltage follower dc output offset voltage shift induced by EMI in the TEM cell IC susceptibility test (circles) and in the direct injection susceptibility tests (rectangles). In both cases the RF source has a frequency of $f = 500$ MHz.
Effect of two orientations into the TEM Cell

Fig. 11. Voltage follower dc output offset voltage shift induced by EMI in the TEM cell IC susceptibility test in the case of the opamp placed in the transverse (circles) and longitudinal orientation (rectangles).
Figure 54
Top View of the TEM Cell with Target Wheel powered by a DC Motor (TLE 4921-3U) for Magnetic Actuation of the Hall IC Samples to be Tested.
• Measurement Method: *Frequency sweeps in steps of 1 MHz at the highest E-field level, remaining one second at each frequency.*

• *In case of malfunction: Decrease of E-field to locate the minimum values.*

• Malfunction Criteria:

• *Missing pulses in the IC output. Jitter of +/- 0.2 ms is exceeded.*
How to control EMC =EMI and EMS

EMITTERS: We must to know the characteristics of time and frequency spectrum
$t_1 > t_2 \text{ and } t_{r1} > t_{r2}$
EMC TYPICAL PROBLEMS

Mainframe

INTRA System EMC

Workstation

CRT SJ

PRINTER

CE
CS
RE
RS
CE
CS
C
C
CS
CE
Incident field coupled with cables and PCB traces.
HOW TO CONTROL EMC?

• Electromagnetic Shielding Design
• Printed Circuit Board (PCB) Design
• Lay-out of Critical Electronic Component
• Filtering Design
ELECTROMAGNETIC SHIELDING

Complete integral shielding of every box and all cables (compartment shielding)

Metal or metalized box

Plastic box

F₁ - F₄ Filters

Shielded cables

Non shielded cables

PCB1

PCB2

PCB3

PS
PCB with one connector - CASE 1

Note: Use separate supplies for the logic families
PCB with one connector - CASE 2

Note: Prevent supply layer overlaps ($V_{CC} / GND$) between the analog and digital area.
POWER SUPPLY AND ELECTRONIC COMPONENTS DISTRIBUTION

- fast digital circuits
- slow digital circuits
- analog circuits

interfaces and line driver circuits

connector

+5V

OV
PCB with one connector - CASE 3

Note:

- Use a “star” supply system for $V_{CC}$ / GND.
- Prevent loops in $V_{CC}$ / GND.
- Prevent loops in clock signal and data lines.
- Keep supply voltage paths for drivers short.
PCB with several connectors

Note:
- Assign logic (interface logic) to the connectors.
- Sort logic according to its purpose.
- Separate logic families.
- Use separate supply systems.
PCB Multilayer Guidelines - CASE 1

IL - Interconnect Layer

**Advantage**
- easy to repair

**Disadvantage**
- radiated emission from IL located outside of the PCB
PCB Multilayer Guidelines - CASE 2

Note:
Direction priority in IL 1 and IL 2 to avoid cross talk.

Advantage
• no radiated emission from signal and data lines

Disadvantages
• not easy to repair
• problems with very fast signals in the inner layers
PCB Multilayer Guidelines - CASE 3

- SH - Shield Layer
- IL - Interconnect Layer
- GND - Ground
- $V_{cc}$ - Supply Layer
Location of decoupling capacitances

decoupling capacitance $D_c$ useless due to $R$ and $L$ in the current path

possible solution with low $R$ and $L$

optimal position of $D_c$

Attn.: multi layer
DECOUPLING CAPACITORS

Wrong:
- Long paths connecting the pins introduce L and C

Right:
- Short paths connecting the pins minimize L and C
Question: What has to be done to meet the EMC requirements in order to get FCC / CE approval?
FILTERING

What to do and what not to do in filter mounting:

a) power mains

b) mains data

c) data

A - unshielded data cable
B - flat cable
C - unshielded connector
What to do and what not to at cable entries:

**d) optimal solution**

- Mains
- Metal or metalized box
- FILTER
- PS
- PCB’s
- F1, F2
- Datafilter
- C1, C2
- Shielded connectors
- PS
- Power supply
• *We must to analyze rightly the EMC Testing Results in order to solve the problems, applying efficiently the available techniques to EMI Control.*

• *We must to select rightly the suppression components, optimizing the installation into the equipment or system, that it must be improved.*
• CMOS operational amplifier: *It presents two main blocks, the first is a fully differential folded cascode with modified input pair and the second is a source cross coupled AB class buffer.*

• *The folded cascode stage and the symmetrical output buffer improve the design in order to achieve intrinsic robustness to interferences and good amplifier performances.*
Block Diagram of the OPAMP
Fig. 2. Schematics of the first stage.
Second Stage Design

Schematics of the second stage.
Fig. 4. Chip microphotograph.
EMI applied to the input pin
EMI applied to the Vdd pin
Offset voltage measurements

EMI applied to the input pin (measurements).

EMI applied to the $V_{dd}$ pin (measurements).
Offset Voltage with EMI applied to the Vss pin

EMI applied to the $V_{ss}$ pin (measurements).
• The offset of new OpAmp is more than one order of magnitude smaller than the uA741, which appears to be rather susceptible to EMI, when the interfering signals are applied to the input pin.

• The offset could easily drive the OpAmp into saturation.
• **Smart power technologies allow the design and realization of complex IC’s composed of analog, digital and power blocks.**

• **In many cases a complete electronic module is collapsed into an IC.**

• **In this devices, interference reach active and passive integrated components by metal interconnection routed on the silicon surface, or through parasitic paths.**
Smart Power Device

Fig. 1 - Top view of a smart power device
Fig. 2 - (a) Lateral PNP bipolar transistor cross-section. (b) PNP transistor in common emitter configuration with substrate interferences (current source) applied to the base terminal by the parasitic capacitor $C_b$. 

Effect of the parasitic capacitance $C_b$
Fig. 3 - Simplified block diagram of the 3845 family ICs
Set-up for RFI Injection on Vcc pin

Fig. 4 – Schematic experimental set-up for RFI injection to VCC pin
Generation of the ungrounded condition

Fig. 5 – Schematic of the experimental set-up for generation of the ungrounded condition
Frequency Shift induced by RFI on Vcc pin

Fig. 6 – Frequency shift induced by RFI on Vcc pin. Signal level = 115dBµV. Nominal duty-cycle = 30%
Duty-cycle shift induced by RFI on Vcc pin.

Fig. 7 – Duty-cycle shift induced by RFI on Vcc pin. Signal level = 115dBμV, Nominal duty-cycle = 30%.
DC Shift induced by RFI on Vcc pin

Fig. 8 – DC shift induced by RFI on Vcc pin. Signal level = 115dBμV, Nominal duty-cycle = 30%. Nominal voltage = 5.1V
DC Shift induced by RFI on Vcc pin

Fig. 9 – DC shift induced by RFI on Vcc pin for component F. Nominal duty-cycle = 30%. Nominal voltage = 5.1 V
Effect of underground condition

Fig. 10 – Effect of underground condition at output pin: $V_{ramp}$ begins to show a discontinuity. From top to bottom: output pin voltage, ramp voltage, secondary side current pulse.
Fig. 11 – Effect of underground condition at output pin: $V_{\text{ramp}}$ resets to zero (B and C type). From top to bottom: output pin voltage; secondary side current pulse; ramp voltage; zoom-out track of the ramp voltage; (a toggle flip flop sets the switching frequency to half the ramp frequency)
Effect of underground condition

Fig. 12 – Effect of underground condition at output pin: the A-type output for an $i_D$ current-peak of nearly 2A. From top to bottom: output pin voltage, secondary side current pulse, ramp voltage.
Effect of underground condition

Fig. 13 – Effect of underground condition at output pin: the F-type presents a blackout in the error-amplifier block that disables the circuit for a long time. From top to bottom: secondary side current pulse, output pin voltage, error amplifier inverting input voltage.
Operational Amplifier – Input stage

Fig. 1 nMOS differential pair
Input Stage robust to EMI

Fig. 2 Double differential pair robust to EMI
Fig. 3 Folded cascode operational amplifier in voltage follower configuration
Output Offset Voltage Induced

Fig. 4 Output offset voltage against RF interference amplitude for interference frequency of 100 MHz

- ○ — usual folded cascode
- ⋆ — modified folded cascode (including double differential stage)
The EMC Standards help us to do measurements of the injected voltages and currents, together with the responses of the ICs tested at controlled conditions, that yield information about the potential immunity of the IC to conducted and radiated RF disturbances in given application.
• MUCHAS GRACIAS!!!!!!!!!!

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